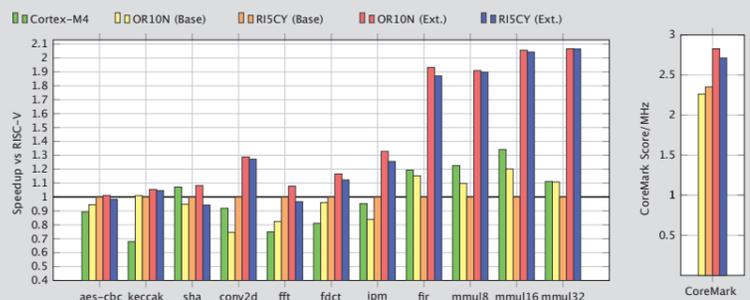


# PULPino: A small single-core RISC-V SoC

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## 1 Introduction

PULPino is an open-source microcontroller-like platform featuring a 32-bit RISC-V core. PULPino evolved from the effort of publishing PULP, the **Parallel Ultra-Low-Power Platform** that is developed as a joint project between ETH Zurich and the University of Bologna, as open-source. Since PULP is a huge project, PULPino has been created as a first-step which re-uses the IPs and cores that were developed for PULP. While the focus for PULP is on extreme energy-efficiency, the spotlight for PULPino is on simplicity and ease of use.



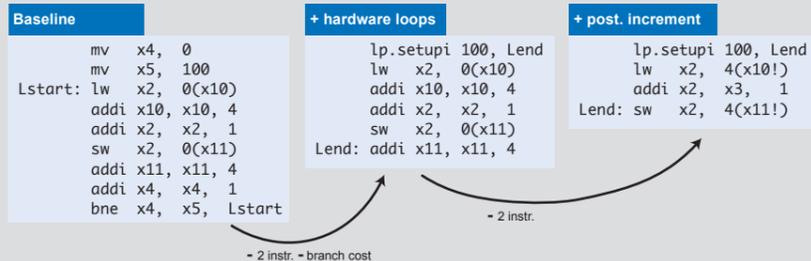
## 2 RI5CY - Signal Processing ISA Extensions

Our goal is to create a platform for low power signal processing, this means tuning the core micro-architecture and the ISA towards this goal. For this purpose we have created non-standard RISC-V instruction set extensions. Those extensions have a low overhead in terms of area and power when they are not in active use. Where those extensions are applicable, they allow for speedups of up to 2x.

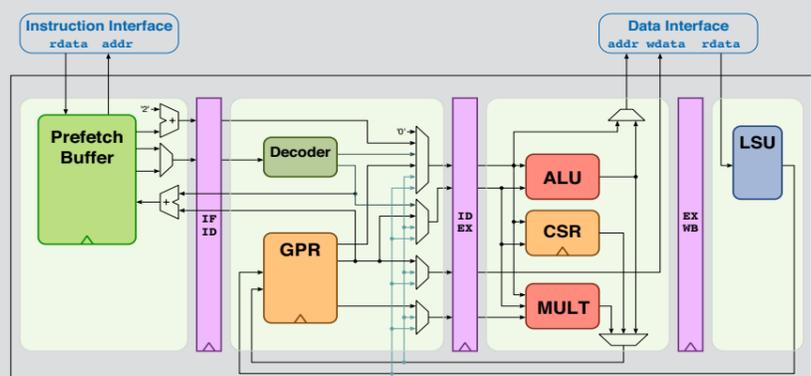
The first set of extensions that were created are hardware loops, post-incrementing load and stores, multiply-accumulate with optional sub-word selection and extensions for the ALU that can perform common operations like minimum, maximum, average and absolute value in one cycle.

### Simple vector addition

```
for (i = 0; i < 100; i++) {
    d[i] = a[i] + 1;
}
```



## 3 RI5CY - Implementation



RI5CY is a simple 4-stage in-order RISC-V core with support for vectorized interrupts on 32 lines, events so that the core can sleep and save energy, exceptions on illegal instructions and memory accesses, basic debug support with software breakpoints and the possibility to use core internal performance counters.

	RI5CY	ARM Cortex M4 <sup>2</sup>	
Technology	65 nm	90 nm	65 nm
Conditions	25°C, 1.2 V	25°C, 1.2 V	25°C, 1.2 V
Dynamic Power [ $\mu$ W/MHz]	17.5	32.82	23.2 <sup>1</sup>
Area [ $\text{mm}^2$ ]	0.050	0.119	0.062 <sup>1</sup>

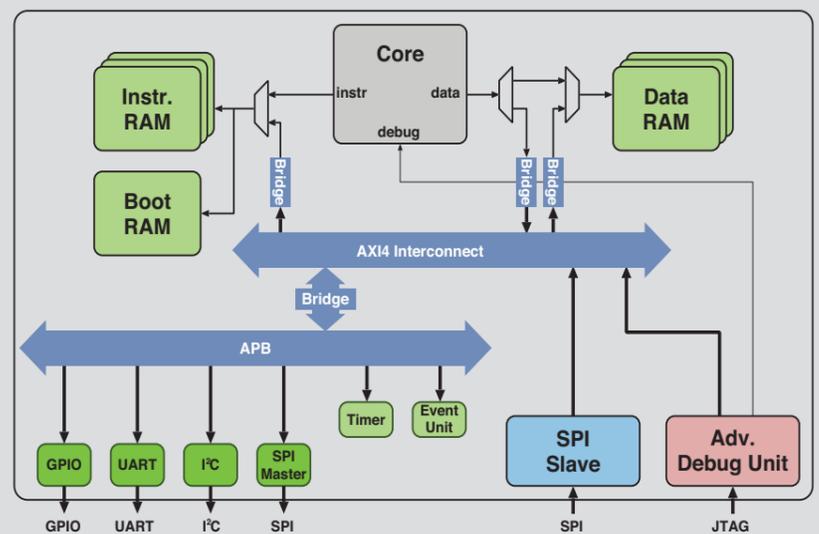
1. scaled from 90nm to 65nm  
2. ARM Cortex M4, <http://www.arm.com/products/processors/cortex-m/cortex-m4-processor.php>

## 4 PULPino

PULPino is a minimal system focused on the core. It has no caches, no memory hierarchy and no DMA. It re-uses the peripherals and the core from the PULP project. It contains an event unit that can put the core to sleep and wake it up when there is an event or interrupt from a peripheral.

To program PULPino the SPI slave or the advanced debug unit can be used. Both have access to the whole memory map and can control PULPino. PULPino can also be used standalone without an external host that controls it. In this mode it starts by using the boot loader contained in the boot ROM in order to load its program from an external SPI flash.

PULPino is available for RTL simulation, FPGA and ASIC. The first tape-out will be done by the end of January in UMC 65 nm technology as a student project.



## 5 Conclusion and Outlook

PULPino is being released open-source under the SolderPad license. The release includes the complete PULPino RTL source, all IPs, the RI5CY core, the environment for RTL simulation and the complete FPGA build flow.

We are currently working on extending the ISA further towards low power signal processing and adding a simple branch predictor to the core. For even easier extensibility and configuration PULPino is currently being ported to IP-XACT.